REMARKS

Applicants hereby traverse the outstanding rejections, and request reconsideration and withdrawal in light of the amendments and remarks contained herein. Claims 1-21 are pending in this application.

Rejection under 35 U.S.C. § 102(e)

Claims 1-21 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ho ('768).

It is well settled that to anticipate a claim, the reference must teach every element of the claim, see M.P.E.P. §2131. Moreover, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he elements must be arranged as required by the claim," see M.P.E.P. § 2131, citing *In re Bond*, 15 US.P.Q.2d 1566 (Fed. Cir. 1990). Furthermore, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim," see M.P.E.P. § 2131, citing Richardson v. Suzuki Motor Co., 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989). Applicants respectfully assert that the rejection does not satisfy these requirements.

Claim 1 defines a method for VLSI chip design that includes "wherein the VLSI chip design is in register transfer language." Similarly, claim 11 defines a VLSI chip whose design was performed according to a method that includes "wherein the design is in register transfer language." Similarly, claim 21 defines a system for forming a VLSI chip design that includes "wherein the VLSI chip design is in register transfer language."

Ho, at least, does not disclose these limitations. More specifically, Ho does not specify that the design in is register transfer language. Ho appears to be silent on this matter. Thus, Ho does not teach all of the claimed limitations. Therefore, the Applicants respectfully assert that for the above reasons claims 1, 11, and 21, are patentable over the 35 U.S.C. § 102 rejection of record.

Claims 2-10 and 12-20 depend directly from base claims 1 and 11, respectively, and thus inherit all limitations of their respective base claims. Each of claims 2-10 and 12-20 sets forth features and limitations not recited by Ho. Thus, the Applicants respectfully asserts that

for the above reasons claims 2-10 and 12-20 are patentable over the 35 U.S.C. § 102 rejection of record.

CONCLUSION

For all the reasons given above, the Applicants submit that the pending claims distinguish over the prior art of record under 35 U.S.C. § 102. Accordingly, the Applicants submit that this application is in full condition for allowance.

Applicants respectfully request that the Examiner call the below listed attorney if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit: October 4, 2002

Typed Name: Kristin Mattern

Signature: K Mattern

Respectfully submitted,

By: _____

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1, 11 and 21 are amended by rewriting as follows:

1. (Amended) A method for VLSI chip design comprising the steps of:

estimating signal routes between functional blocks;

determining resistance and capacitance values for the estimated signal routes; and

building a model of said signal routes including resistance and capacitance values;

wherein the VLSI chip design is in register transfer language.

11. (Amended) A VLSI chip whose design was performed according to a method comprising the steps of:

estimating signal routes between functional blocks;

determining resistance and capacitance values for the estimated signal routes; and

building a model of said signal routes including resistance and capacitance values;

wherein the design is in register transfer language.

21. (Amended) A system for forming a VLSI chip design comprising:

means for estimating signal routes between functional blocks;

means for determining resistance and capacitance values for the estimated signal routes; and

means for building a model of said signal routes including resistance and capacitance values;

wherein the VLSI chip design is in register transfer language.